

SRAM CELL WITH HORIZONTAL MERGED DEVICES

Abstract of the Disclosure

A merged structure SRAM cell is provided that includes a first transistor and
5 a second transistor. The second transistor gate forms a load resistor for the first
transistor and the first transistor gate forms a load resistor for the second transistor.
Also provided is a method of reading a memory cell that comprises applying a
potential difference (V_{DIFF}) to a selected memory cell by providing a column line
potential (V_{C}) and a row line potential (V_{R}). According to this method, V_{DIFF} is
10 increased by an increment less than a transistor threshold voltage (V_{T}). It is then
determined whether the increased V_{DIFF} results in a current flow on the column line
for the selected memory cell. Also provided is a method of writing a memory cell
that comprises applying V_{DIFF} and increasing V_{DIFF} by an increment more than V_{T} to
set the selected memory cell to a one state.

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